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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/845,881	04/30/2001	Quat T. Vu	884.384US1	4041

21186 7590 04/14/2004

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EXAMINER	
SARKAR, ASOK K	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 04/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/845,881	VU ET AL.	
	Examiner	Art Unit	
	Asok K. Sarkar	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 January 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-26* is/are allowed.

6)☒ Claim(s) *1-7 and 9* is/are rejected.

7)☒ Claim(s) *8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/15/03; 1/6/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *PTO-1449 filed 4/5/2004*.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on December 15, 2003 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1 – 4, 6, 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bertolet, US 5,844,317.

Regarding claim 1, Bertolet teaches a microelectronic device comprising:

- a microelectronic die 50 having a plurality of bond pads 100 on an active surface thereof with reference to Fig. 7;
- an interfacial metal layer 90 deposited over said active surface of said microelectronic die 50,
- said interfacial metal layer having at least one conductive element that is conductively coupled to multiple bond pads 100 on said active surface of said microelectronic die to provide signal distribution between points within said microelectronic die with reference to Fig. 7 in columns 11 and 12.

Bertolet teaches packaged microelectronic devices in the background section in columns 1 and 2 especially in column 2, lines 33 – 43 for the benefit of providing wire bondable packages, but fails to teach microelectronic die being fixed within an opening in a package core.

However, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Bertolet's teaching and fix the microelectronic die within

an opening in a package core for the benefit of providing wire bondable packages as taught by Bertolet in column 2, lines 33 – 43.

Regarding claim 2, Bertolet teaches a at least one build up metallization layer 190 deposited over said interfacial metal layer 90, said at least one build up metallization layer 190 being conductively coupled to said interfacial metal layer 90 through a dielectric layer 140 having a plurality of via holes with respect to Fig. 7.

Regarding claim 3, Bertolet teaches least one conductive element 90 includes a first pad that is directly coupled to a first bond pad on said active surface of said microelectronic die, a second pad that is directly coupled to a second bond pad on said active surface of said microelectronic die, and a conductive trace portion connecting said first and second pads with reference to Figs. 7 and 8.

Regarding claim 4, Bertolet teaches making electrical connections to the semiconductor device with wire bonding in column 1, lines 10 – 17, but fails to teach at least one conductive element is configured to receive a signal from a first bond pad on said active surface of said microelectronic die during operation of said microelectronic device to transfer signal to a second bond pad on said active surface of said microelectronic die.

However, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Bertolet's teaching and configure the conductive element to receive a signal from a first bond pad on said active surface of said microelectronic die during operation of said microelectronic device to transfer signal to a second bond pad on said active surface of said microelectronic die for the benefit of operating the

packaged die with electrical connections as taught by Bertolet in column 1, lines 33 – 43.

Regarding claim 6, Bertolet fails to teach package core of metal material. However, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Bertolet's teaching and provide a metal material for package core for the benefit of providing efficient heat sink and cooling operations.

Regarding claim 7, Bertolet teaches a passivation layer 80 with reference to Fig. 7.

Regarding claim 9, Bertolet fails to teach an encapsulation material for packaging. However, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Bertolet's teaching and use an encapsulation material for the benefit of protecting the die from harsh external atmosphere.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bertolet, US 5,844,317 in view of Perino, US 6,621,155.

Bertolet fails to teach the microelectronic die includes a clock source to provide a clock signal to a first bond pad on the active surface, wherein the interfacial metal layer includes a conductive element that is conductively coupled to the first bond pad and to a plurality of other bond pads on said active surface to distribute the clock signal to the plurality of other bond pads.

Perino teaches a microelectronic die providing clock source to provide a clock signal to a first bond pad on the active surface, wherein the interfacial metal layer includes a conductive element that is conductively coupled to the first bond pad and to a

plurality of other bond pads on said active surface to distribute the clock signal to the plurality of other bond pads with reference to Figs. 7A and 7B for the benefit of providing space saving for system layout in column 1, lines 31 – 37.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Bertolet's teaching and provide clock source to provide a clock signal to a first bond pad on the active surface, wherein the interfacial metal layer includes a conductive element that is conductively coupled to the first bond pad and to a plurality of other bond pads on said active surface to distribute the clock signal to the plurality of other bond pads for the benefit of providing space saving for system layout as taught by Perino in column 1, lines 31 – 37.

Allowable Subject Matter

7. Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claims 10 – 26 are allowed.

9. The following is an examiner's statement of reasons for allowance:

Claims 10 – 19 recite, inter alia, a microelectronic device comprising an interfacial metal layer having plurality of separate conductive elements including at least one separate conductive element that is conductively coupled to multiple bond pads. The art of record does not disclose or anticipate the above limitation in combination with other claim elements nor would it be obvious to modify the art of record so as to form a device including the above limitation.

Claims 20 – 26 recite, inter alia, a microelectronic device comprising an interfacial metal layer having a first single conductive element coupled to multiple bond pads and to both first bond pad of first die and a second bond pad of a second die. The art of record does not disclose or anticipate the above limitation in combination with other claim elements nor would it be obvious to modify the art of record so as to form a device including the above limitation.

Conclusion

10. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 571 272 1970. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Asok Kumar Sarkar

Asok K. Sarkar
April 5, 2004

Patent Examiner